METHOD TO INVERT THE RESISTANCE DRIFT OF AMORPHOUS CHALCOGENIDES

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HINTERGRUND

Resistive switches for memory storages are realized by phase change materials (PCMs) that exhibit a large electrical and optical contrast between the amorphous and the crystalline phase. This property difference and the ability to switch abruptly and reversibly is exploited in commercial binary data storage such as Intel Optane. The difference in properties between the two phases is so large that by varying the amorphous and crystalline volume fractions in a memory cell, multi-level data storage (MLS) is made possible. MLS allows for in-memory computing in machine learning algorithms and storing synaptic weights in a single memory cell in neuromorphic computing. However, the amorphous phase of chalcogenides, including PCMs, shows a steady increase in resistance , a phenomenon oftentimes referred to as -drift. This drift causes MLS devices to fail to read correctly after a certain time interval, which has so far hindered the commercialization of PCM-based MLS devices for machine learning and neuromorphic computing.

LÖSUNG

Our invention focusses on a solution to the main problem of the resistance drift and how to restore the originally programmed resistance value of the memory cell. We found that the resistance drift is caused by structural relaxation of the glassy (amorphous) phase in chalcogenides, including the technologically important group of PCMs. When the temperature is raised above the glass transition temperature prior to readout, the glass transitions to the physical state of the undercooled liquid (still amorphous), eliminating the thermal history of the glassy state. When the chalcogenide is then cooled to room or operating temperature, a new glassy state forms that has not yet experienced significant -drift. Applying -recovery at lowest possible temperature and for the shortest possible durations ensures that the volume fractions of the amorphous and crystalline phase in the memory cell change only unnotably during the -recovery temperature pulse. Thus, the originally programmed resistance state of the memory cell is recovered.

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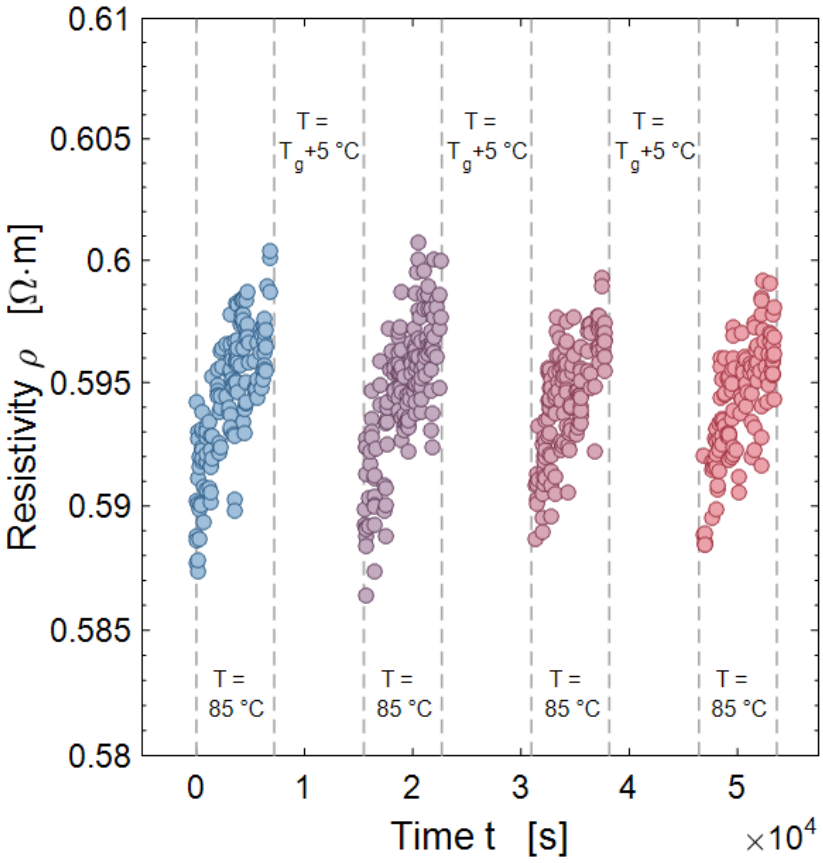
ENTWICKLUNGSSTAND

Machbarkeit

CATEGORIES

//Elektronik und Elektrotechnik



VORTEILE

- Resistance drift is inverted and the originally programmed state of the PCM memory cell is recovered.
- No major changes to the PCM- or chalcogenide-memory cell design mandatory.
- Only minor adaptations to the electrical control/writing circuit required.
- Our invention enables the commercialization of PCM-based multi-level data storage required for machine learning, neuromorphic computing and artificial intelligence, while being easy to implement to existing designs.

SERVICE

- German and international patent application pending
- Figure 1 shows the proof of the concept: At an operating temperature of 85 °C, the resistance is drifting (increasing) continuously. Raising the temperature to above the glass transition temperature and cooling back to 85 °C removes the drifted resistance and recovers the initial resistance level repeatedly.
- We offer a new and easy to implement temperature pre-readout pulse that recovers the originally programmed resistance value in a binary or multi-level PCM-based data storage cell.
- We are looking for partners of patent exploitation in prototyping and a subsequent up-scaling in a joint development with an industry partner.