EBERHARD KARLS
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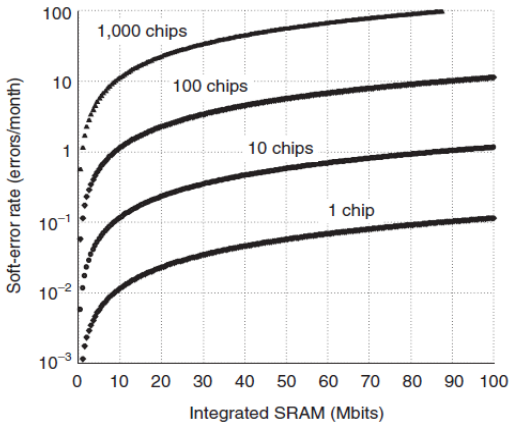
Efficient Hardware-Based Real-time Forward Error Correction for Safety-Critical Applications

Technology Description



Monthly system soft error rate as a function of the number of chips in the system and the amount of embedded SRAM per chip.

Quelle: R. Baumann, "Soft Errors in Advanced Computer Systems", http://doi.ieeecomputersociety.org/10.1109/MDT.2005.69

Real-time control of safety-critical applications is becoming increasingly important in a variety of markets as the automotive, aviation, financial or medical sector. Furthermore, with electronic components becoming smaller and more complex, the hardware immanent error probability arises.

We present a robust and reliable forward error correction technique enabling data transmission in noisy environments. Our mathematically proved decoder corrects single-bit and multi-bit errors in real-time.
It can be easily realized on hardware level in embedded systems: A simple non-clocked combinational circuit consisting of only a few logic gates performs the decoding. Registers or flip-flops are not needed. The decoder works for a wide variety of block codes. This allows the code characteristics like block size and correctable errors to be tuned to your individual needs.

Innovation

Up to now: On hardware level, only single-bit or very complex and expensive multi-bit error correction.

Now: Real-time single- and multi-bit error correction on hardware level in embedded systems with only a few logic gates.

Applications

Electronic safety and industrial control systems in

- Automotive electronics, e.g. advanced driver assistance systems
- Avionics
- Enterprise Computing, e.g. error correction on memory and storage devices
- Medical engineering

Advantages

- Only very few and simple electronic components needed.
- Realtime multi-bit error correction.
- Code parameters like block size and maximal number of correctable errors adjustable.
- No clock signal required, no flip-flops used.

Proof of Concept

Prototype (CPLD).
More information is located on the back.

Requested Cooperation

Licensing partners.
Patent granted. Priority Date: 2013-02-01

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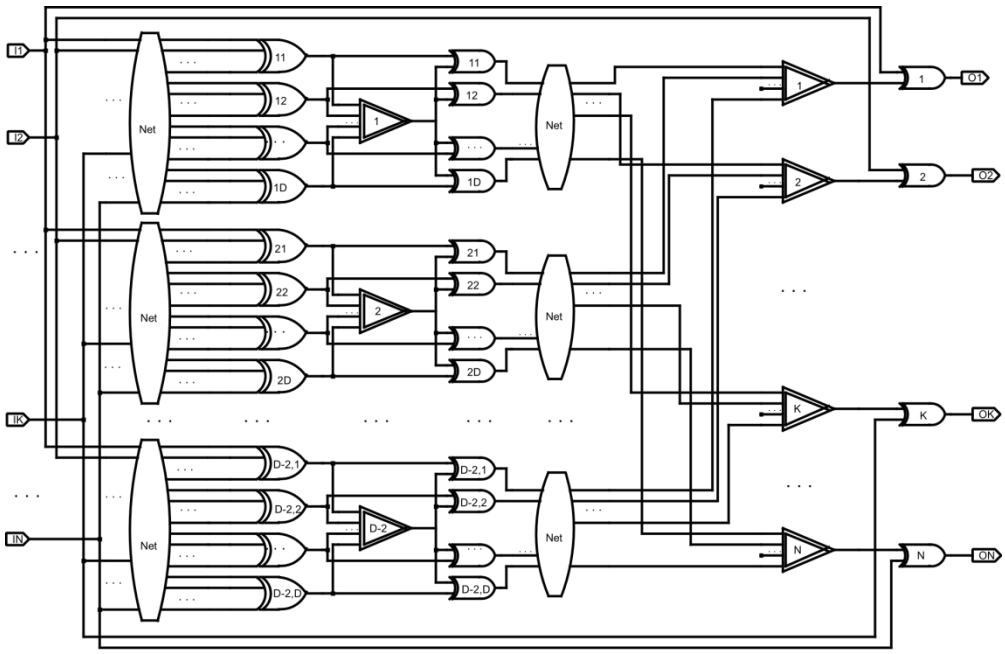
Further Information about the New Decoder

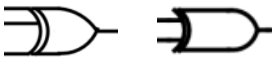
General Schematic of the New Decoder

The new decoder consists of three layers of modulo-2-adders and two layers of majority gates.



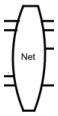
N = Code block size
K = Information size
T = Correctable errors per block
D = Minimum distance

Modulo-2-adder



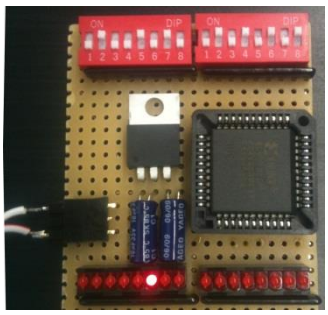
Majority gate

Fixed wiring without logic gates



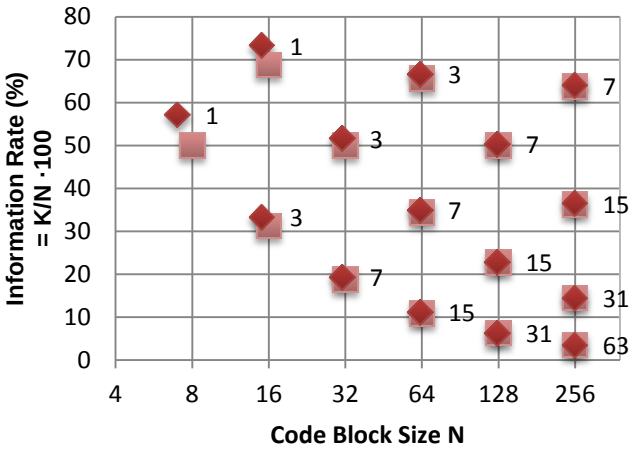
Prototype

The decoder has been realized on a CPLD for a [N=16, K=11, T=5] code to demonstrate correctness and reliability of our decoding algorithm.



A Wide Choice of Code Parameters

The new decoder is applicable to a wide range of codes. The chart and the table on the right-hand side display how many errors our decoder is capable to correct depending on the chosen block size and information rate.



N	K	T
7 or 8	4	1
15 or 16	5	3
	11	1
31 or 32	6	7
	16	3
63 or 64	7	15
	22	7
	42	3
127 or 128	8	31
	29	15
	64	7
255 or 256	9	63
	37	31
	93	15
	163	7

Electronic Components

For selected codes, the number of required components is listed in the table below distinguishing the number of inputs.

N, K, T	15, 11, 1	16, 11, 1	31, 16, 3	32, 16, 3	63, 42, 3	64, 42, 3
Modulo-2-Adder	18 x 9 x	19 x 8 x	65 x 49 x	64 x 48 x	91 x 9 x	90 x 48 x
Majority	11 x 3 x	11 x 2 x	16 x 7 x	16 x 6 x	42 x 7 x	42 x 6 x